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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/535,591	05/19/2005	Jan-Willem Van De Waerdt	US02 0465 US	7635

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EXAMINER	
CYGIEL, GARY W	
ART UNIT	**PAPER NUMBER**
2187	

NOTIFICATION DATE	DELIVERY MODE
10/05/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/535,591	VAN DE WAERDT ET AL.	
	Examiner	Art Unit	
	GARY W. CYGIEL	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 June 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 4-8, 10-14, 16-18 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Sherwood et al. (NPL:Predictor-Directed Stream Buffers) (hereinafter referred to as Sherwood).

Consider **Claim 1**,

Sherwood teaches a method of data retrieval comprising the steps of:

providing a first memory circuit (Sherwood:Fig 3);

providing a stride prediction table (SPT) that is indexed with cache line miss information (Sherwood:Fig 3, Sec 4.2, load-PC (for a missed load) is used to index into the stride table. Page 9:Left Column:Lines 1-3,only cache block addresses are used.);

providing cache memory circuit (Sherwood:Fig 3);

executing instructions for accessing data within the first memory (Instructions must be executed to access data within the first memory.);

detecting a cache miss (Sherwood:Sec 4.3 ¶3, detects two cache misses in a row); and

only allowing accesses to the SPT in response to a detection of a cache miss (Sherwood:Sec 4.2/4.3; see also Response to Arguments below, section **[A]**.);and

only allowing updates to the SPT in response to the detection of a cache miss. (Sherwood:Sec 4.2/4.3).

Consider **Claims 2 and 16**,

Sherwood further teaches wherein the cache memory circuit is a stream buffer (Sherwood:Fig 3).

Consider **Claim 4**,

Sherwood further teaches wherein the cache memory circuit and the SPT are within a same physical memory space (Sherwood:Fig 3).

Consider **Claim 5**,

Sherwood further teaches wherein the first memory is an external memory circuit separate from a processor executing the instructions (Sherwood:Fig 3,data line from/to next lower level of memory.).

Consider **Claims 6 and 7**,

Sherwood further teaches wherein the step of detecting a cache miss includes the steps of:

determining whether an instruction to be executed by the processor is a memory access instruction;

when the instruction is a memory access instruction, determining whether data at a memory location of the memory access instruction is present within the cache; and,

when the data is other than present within the cache, detecting a cache miss, and accessing and updating the SPT only when the cache miss has occurred (Sherwood:Sec 4.3 ¶3, a cache miss occurs when a requested memory line is not in the cache, therefore requiring the first two limitations of these claims.).

Consider **Claim 8**,

Sherwood further teaches wherein the step of allowing access provides a step of filtering that prevents unnecessary access and updates to entries within the SPT (Sherwood:Sec 4.3).

Consider **Claim 10**,

Sherwood further teaches wherein the SPT comprises an address field, and where a size of the address field is less than an address space used to index the SPT (Sherwood:Sec 4.2 ¶3, SPT stores the last address for the load. Page 9:Left Column:Lines 1-3,only cache block addresses are used and *not* the full address.).

Consider **Claim 11**,

Sherwood teaches an apparatus comprising:

a stride prediction table (SPT) that is indexed with cache line miss information (Sherwood:Fig 3, Sec 4.2, load-PC (for a missed load) is used to index into the stride table. Page 9:Left Column:Lines 1-3,only cache block addresses are used.); and

a filter circuit for use with the SPT, the filter circuit preventing both accesses and updates to the SPT unless a cache miss is detected (Sherwood:Sec 4.2/4.3; see also Response to Arguments below, section **[A]**.).

Consider **Claim 12**,

Sherwood further teaches a memory circuit, the memory circuit for storing the SPT therein (Sherwood:Fig 3).

Consider **Claim 13**,

Sherwood further teaches a cache memory, the cache memory residing within the memory circuit (Sherwood:Fig 3).

Consider **Claim 14**,

Sherwood further teaches wherein the memory circuit is a single ported memory circuit (Sherwood:Fig 3, Page 5, paragraph labeled prediction, only one request can be processed at a time.)

Consider **Claim 17**,

Sherwood teaches a method of data retrieval comprising the steps of:

providing a first memory circuit (Sherwood:Fig 3);

providing a stride prediction table (SPT) that is indexed with cache line miss information (Sherwood:Fig 3, Sec 4.2, load-PC (for a missed load) is used to index into the stride table. Page 9:Left Column:Lines 1-3,only cache block addresses are used.);

providing cache memory circuit (Sherwood:Fig 3);

executing instructions for accessing data within the first memory (Instructions must be executed to access data within the first memory.);

detecting a cache miss (Sherwood:Sec 4.3 ¶3, detects two cache misses in a row); and

restricting accesses to the SPT in response to the detection of a cache miss (Sherwood:Sec 4.2/4.3; see also Response to Arguments below, section **[A]**.).

Consider **Claim 18**,

Sherwood further teaches wherein the step of restricting provides a step of filtering that prevents unnecessary access and updates to entries within the SPT (Sherwood:Sec 4.2/4.3).

Consider **Claim 20**,

Sherwood further teaches wherein the SPT comprises an address field, and where a size of the address field is less than an address space used to index the SPT (Sherwood:Sec 4.2 ¶3, SPT stores the last address for the load. Page 9:Left Column:Lines 1-3,only cache block addresses are used and *not* the full address.).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 3, 9, 15 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sherwood et al. (NPL:Predictor-Directed Stream Buffers) (hereinafter referred to as Sherwood) in view of Handy (NPL: the Cache Memory book) (hereinafter referred to as Handy).

Consider **Claim 3, 9, 15 and 19**,

Sherwood teaches a method according to claim 1 or 13 respectively, but does not specifically disclose all the details regarding the circuits construction.

Handy does teach these limitations such as:

wherein the cache memory circuit is a random access cache memory (Handy:Page 28, SRAM cell used in internal cache.).

wherein the cache memory circuit is integral with the processor executing the instructions (Handy:Page 28, CPU on same chip as on-chip cache.).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to implement the circuit construction concepts as taught by Handy in the system of Sherwood because they are notoriously well known concepts in the art. The use of these methods constitutes only design choice and has no novelty in the art.

Response to Arguments

6. Applicant's arguments filed 10 June 2009 have been fully considered but they are not persuasive.

[A] Re: SPT is accessed independent of a cache miss.

The applicant argues that the SPT is accessed each cycle and is therefore accessed outside of a cache miss and thus fails to correspond to the limitations of the independent claims. The applicant appears to be confusing the address based Markov table and the PC based stride table (stride prediction table). Section 4.2 (3rd paragraph) states “In the write-back stage, the load-PC (for a missed load) is used to index into the stride table." The very information used to index into the stride prediction table (PC based stride table) comes from a cache *miss*. The information to index into (access) the stride prediction table of the SFM (stride filtered Markov predictor) is generated

upon a cache miss, therefore it is not clear why the applicant continues to assert that the SPT of the SFM is accessed each cycle.

The applicant again argues that the SPT is accessed every cycle, but continues to quote a portion of Sherwood that describes a related, but different, system compared to the Stride Filtered Markov (SFM) predictor relied upon by the examiner. The SFM predictor (Sherwood:Fig 3:Sec 4.2/4.3) is different than the predictor directed stream buffer implementation (Sherwood:Fig 2:Sec 4.1). Sherwood further describes that the SFM predictor provides different and uniformly better results than other address predictors (Sherwood:Page 5:Sec 4.1, under heading "lookup.").

Conclusion

1. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GARY W. CYGIEL whose telephone number is (571)270-1170. The examiner can normally be reached on Tuesdays and Thursdays 12:00pm-2:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Christian Chace can be reached on (571)272-4190. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Gary W Cygiel/
Examiner, Art Unit 2187

/G. W. C./
Examiner, Art Unit 2187
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